100/40 Gbps Ethernet - Are you ready?

PMD LAYER

The **Physical Medium Dependent** sublayer or **PMD** defines the details of transmission and reception of individual bits on the physical medium. The PMD layer interfaces with the PMA layer and translates the encoded data to and from signals suitable for the physical medium. The PMA continuously sends parallel bit streams to the PMD, one per lane. The PMD converts these streams of bits into separate optical signal streams; the optical signal streams are then wavelength division multiplexed and delivered to the Medium Dependent Interface (MDI).
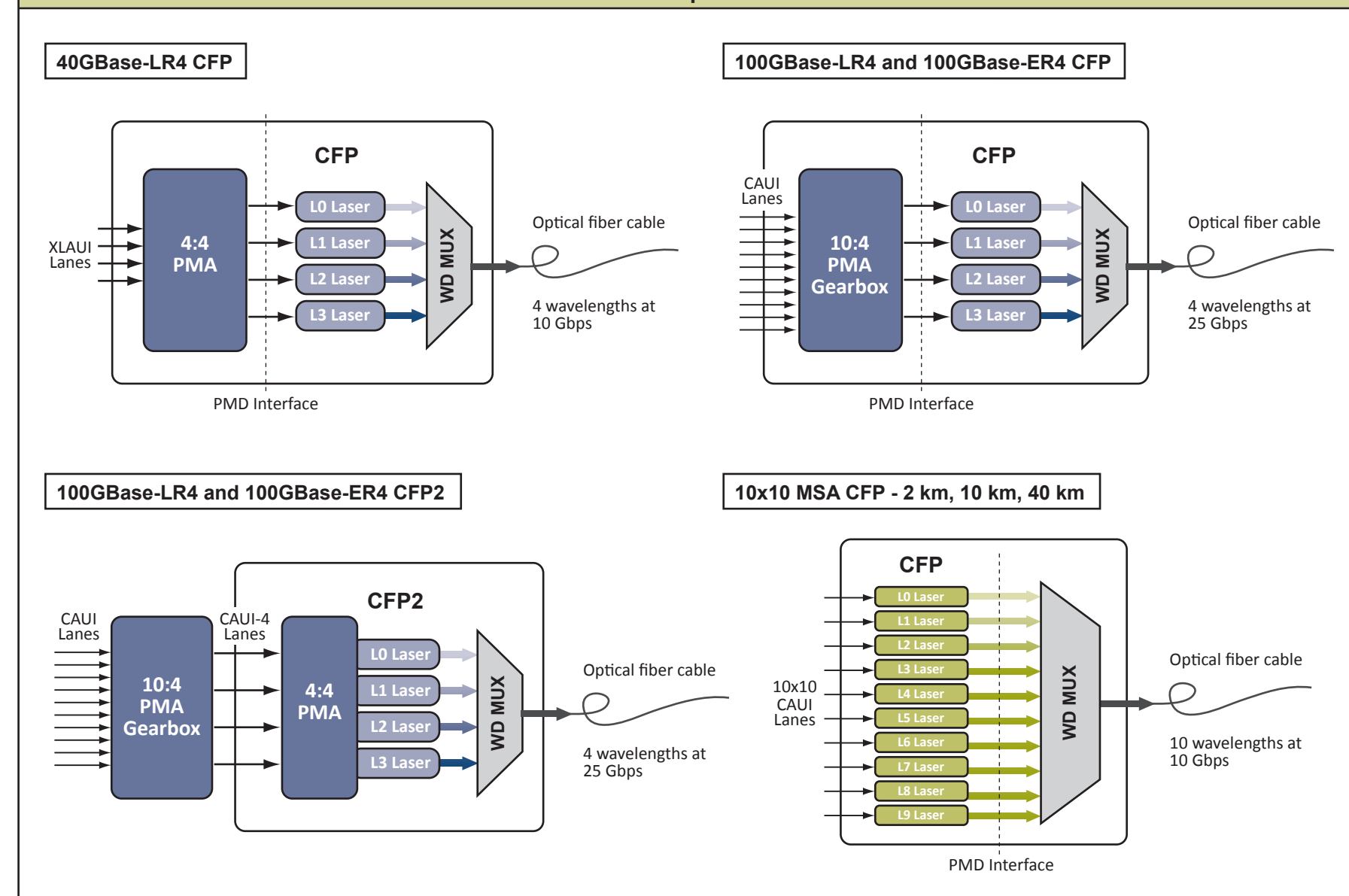
CFP Types

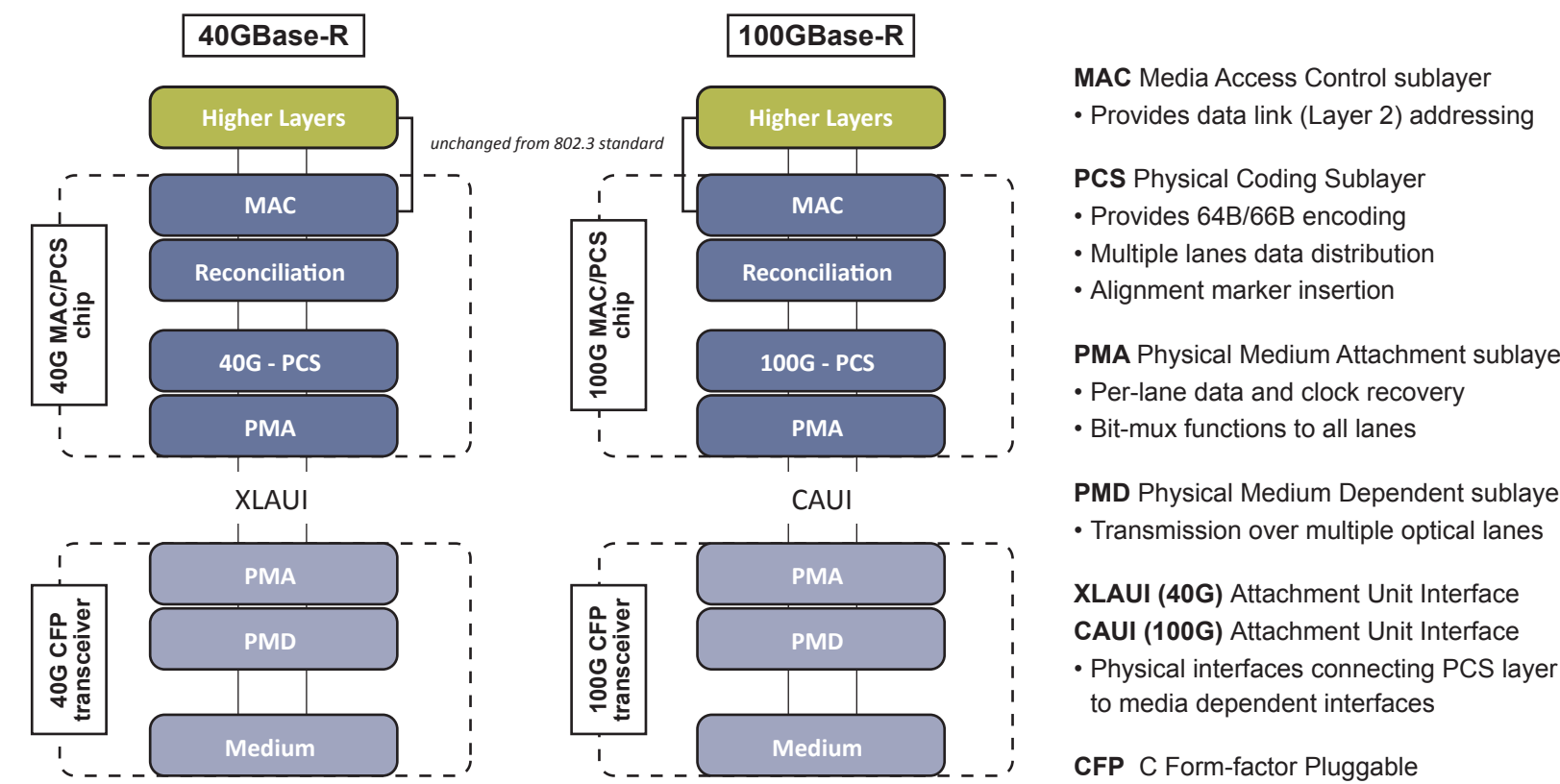|	40GBase-LR4	100GBase-SR10	100GBase-LR4	100GBase-ER4	10x10 - 2 km	10x10 - 10 km	10x10 - 40 km
Standard	IEEE 802.3ba	IEEE 802.3ba	IEEE 802.3ba	IEEE 802.3ba	10x10 MSA	10x10 MSA	10x10 MSA
Wavelength	1310 nm WDM ITU-T G.694.2	850 nm (10 fiber pairs)	1310 nm WDM ITU-T G.694.1	1310 nm WDM ITU-T G.694.1	1550 nm WDM	1550 nm WDM	DWDM ITU-T G.694.1
Reach	10 km	150 m	10 km	40 km	2 km	10 km	40 km
Optical rate	4 x 10 Gbps	10 x 10 Gbps	4 x 25 Gbps	4 x 25 Gbps	10 x 10 Gbps	10 x 10 Gbps	10 x 10 Gbps

WDM Lane Assignments

Lane	Center Wavelength (nm) 40GBase-LR4	Center Wavelength (nm) 100GBase-LR4 100GBase-ER4	Center Wavelength (nm) 10x10 MSA - 2 km 10x10 MSA - 10 km	Center Frequency (THz) 10x10 MSA - 40 km Band 1	Band 2	Band 3	Band 4	Band 5	Band 6	Band 7	Band 8
L0	1271	1295.56	1523	196.10	195.00	193.90	192.80	196.05	194.95	193.85	192.75
L1	1291	1300.05	1531	196.00	194.90	193.80	192.70	195.95	194.85	193.75	192.65
L2	1311	1304.58	1539	195.90	194.80	193.70	192.60	195.85	194.75	193.65	192.55
L3	1331	1309.14	1547	195.80	194.70	193.60	192.50	195.75	194.65	193.55	192.45
L4	n/a	n/a	1555	195.70	194.60	193.50	192.40	195.65	194.55	193.45	192.35
L5	n/a	n/a	1563	195.60	194.50	193.40	192.30	195.55	194.45	193.35	192.25
L6	n/a	n/a	1571	195.50	194.40	193.30	192.20	195.45	194.35	193.25	192.15
L7	n/a	n/a	1579	195.40	194.30	193.20	192.10	195.35	194.25	193.15	192.05
L8	n/a	n/a	1587	195.30	194.20	193.10	192.00	195.25	194.15	193.05	191.95
L9	n/a	n/a	1595	195.20	194.10	193.00	191.90	195.15	194.05	192.95	191.85

CFP Options

40GBase-LR4 CFP

100GBase-LR4 and 100GBase-ER4 CFP

100GBase-LR4 and 100GBase-ER4 CFP2

10x10 MSA CFP - 2 km, 10 km, 40 km

IEEE 802.3ba STANDARD
Protocol Stack

MAC Media Access Control sublayer
• Provides data link (Layer 2) addressing

PCS Physical Coding Sublayer
• Provides 64B/66B encoding
• Multiple lanes data distribution
• Alignment marker insertion

PMA Physical Medium Attachment sublayer
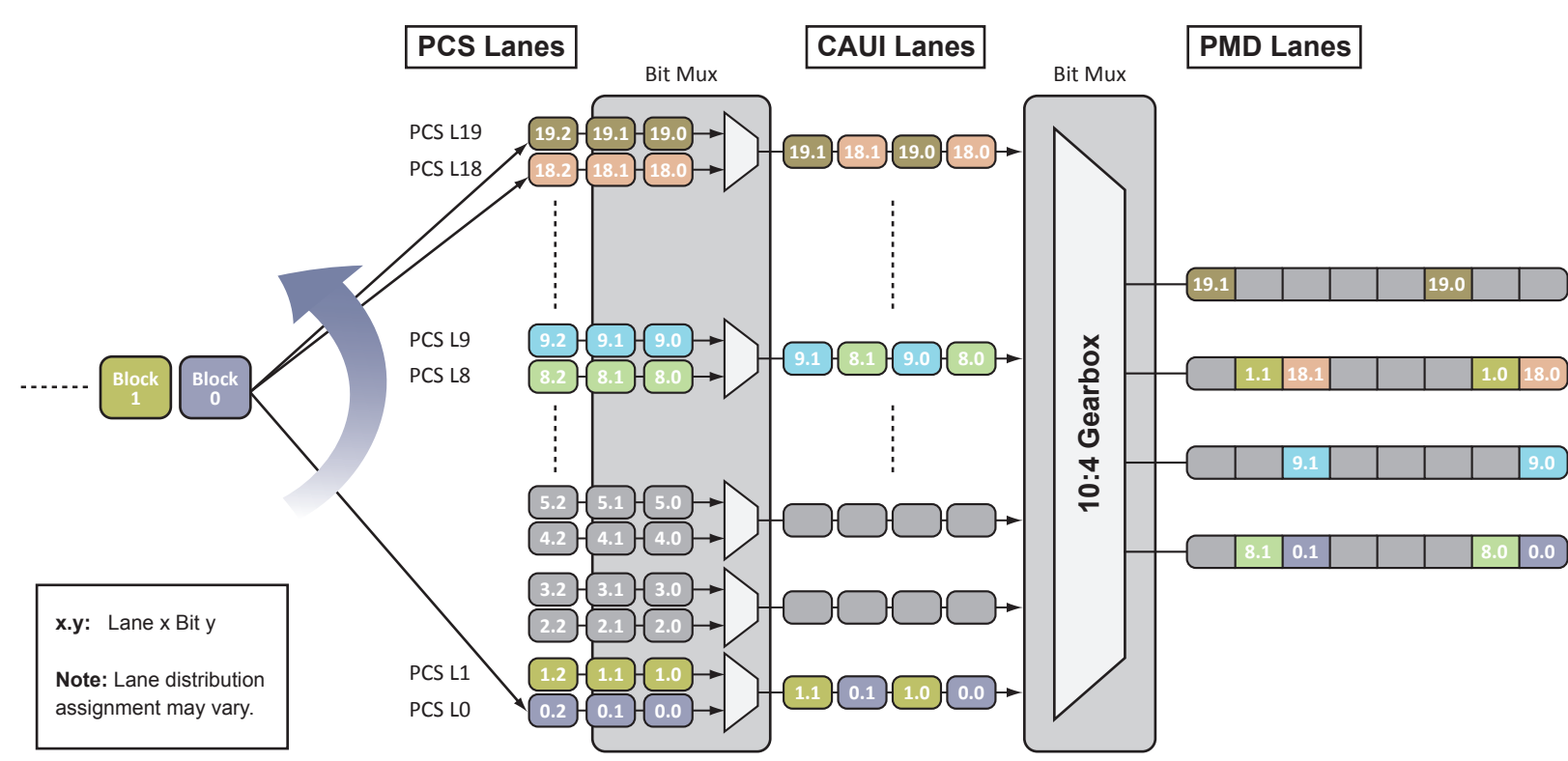• Per-lane data and clock recovery
• Bit-mux functions to all lanes

PMD Physical Medium Dependent sublayer
• Transmission over multiple optical lanes

XLAUI (40G) Attachment Unit Interface
CAUI (100G) Attachment Unit Interface
• Physical interfaces connecting PCS layer to media dependent interfaces
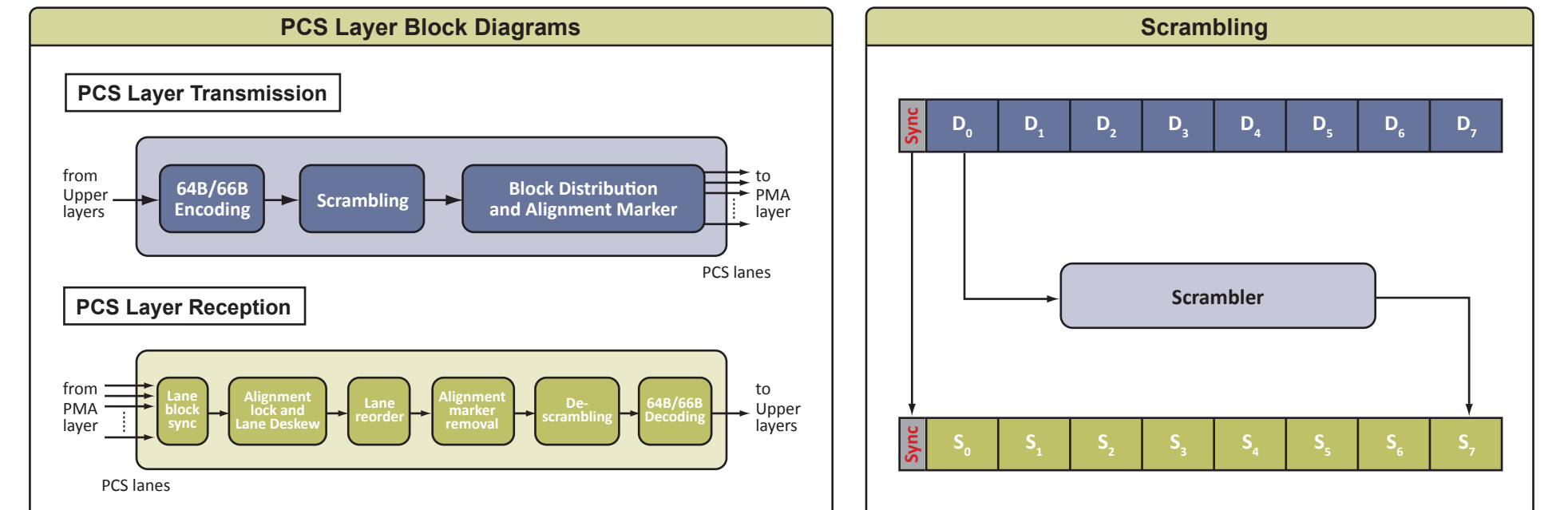
CFP C Form-factor Pluggable

THE BIG PICTURE
100GBase-R

x.y: Lane x Bit y

Note: Lane distribution assignment may vary.

PMA LAYER

The **Physical Medium Attachment** sublayer or **PMA** allows the PCS to connect in a media-independent way with a range of physical media. It uses bit level multiplexing to adapt the PCS lanes to the appropriate number of physical lanes required by the PMD interface.

PCS to CAUI Lanes Bit Mux
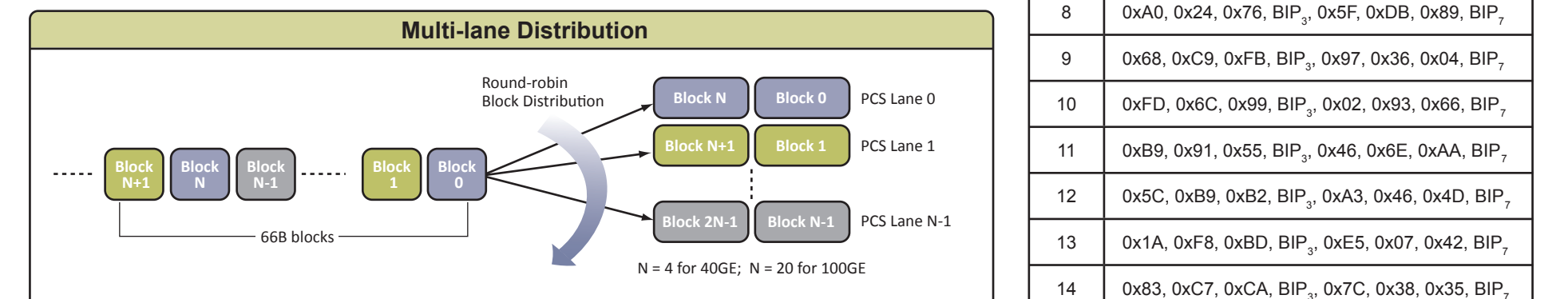

40GBase-LR4

100GBase-LR4/ER4

PCS LAYER

The **Physical Coding Sublayer (PCS)** shields upper layers (MAC) from the specific nature of the underlying channel. Both 40GBase-R and 100GBase-R are based on a 64B/66B code which supports transmission of data and control characters, while maintaining robust error detection. When communicating with the lower layer (PMA), the PCS uses multiple serial streams or PCS lanes.

PCS Layer Block Diagrams

PCS Layer Transmission

PCS Layer Reception

Scrambling

64B to 66B Blocks Encoding

Alignment Marker Format

Multi-lane Distribution

N = 4 for 40GE; N = 20 for 100GE

Alignment Marker Encoding

40GBase-R *

Lane	Encoding $\{M_0, M_1, M_2, BIP_3, M_4, M_5, M_6, BIP_7\}$
0	0x90, 0x76, 0x47, BIP_3, 0x6F, 0x89, 0x88, BIP_7
1	0xF0, 0xC4, 0xE6, BIP_3, 0x0F, 0x3B, 0x19, BIP_7
2	0xC5, 0x65, 0x9B, BIP_3, 0x3A, 0x9A, 0x64, BIP_7
3	0xA2, 0x79, 0x3D, BIP_3, 0x5D, 0x86, 0xC2, BIP_7

100GBase-R *

Lane	Encoding $\{M_0, M_1, M_2, BIP_3, M_4, M_5, M_6, BIP_7\}$
0	0xC1, 0x68, 0x21, BIP_3, 0x3E, 0x97, 0xDE, BIP_7
1	0x9D, 0x71, 0x8E, BIP_3, 0x62, 0x8E, 0x71, BIP_7
2	0x59, 0x4B, 0xE8, BIP_3, 0xA6, 0xB4, 0x17, BIP_7
3	0x4D, 0x95, 0x7B, BIP_3, 0xB2, 0x6A, 0x84, BIP_7
4	0xF5, 0x07, 0x09, BIP_3, 0x0A, 0xF8, 0xF6, BIP_7
5	0xDD, 0x14, 0xC2, BIP_3, 0x22, 0xEB, 0x3D, BIP_7
6	0x9A, 0x4A, 0x26, BIP_3, 0x65, 0xB5, 0xD9, BIP_7
7	0x7B, 0x45, 0x66, BIP_3, 0x84, 0xBA, 0x99, BIP_7
8	0xA0, 0x24, 0x76, BIP_3, 0x5F, 0xDB, 0x89, BIP_7
9	0x68, 0xC9, 0xFB, BIP_3, 0x97, 0x36, 0x04, BIP_7
10	0xFD, 0x6C, 0x99, BIP_3, 0x02, 0x93, 0x66, BIP_7
11	0xB9, 0x91, 0x55, BIP_3, 0x46, 0x6E, 0xAA, BIP_7
12	0x5C, 0xB9, 0xB2, BIP_3, 0xA3, 0x46, 0x4D, BIP_7
13	0x1A, 0xF8, 0xBD, BIP_3, 0xE5, 0x07, 0x42, BIP_7
14	0x83, 0xC7, 0xCA, BIP_3, 0x7C, 0x38, 0x35, BIP_7
15	0x35, 0x36, 0xCD, BIP_3, 0xCA, 0xC9, 0x32, BIP_7
16	0xC4, 0x31, 0x4C, BIP_3, 0x3B, 0xCE, 0xB3, BIP_7
17	0xAD, 0xD6, 0xB7, BIP_3, 0x52, 0x29, 0x48, BIP_7
18	0x5F, 0x66, 0x2A, BIP_3, 0xA0, 0x99, 0xD5, BIP_7
19	0xC0, 0xF0, 0xE5, BIP_3, 0x3F, 0x0F, 0x1A, BIP_7

*Alignment marker is inserted after every 16383 66B blocks on each PCS lane.

PCS Alarms and Errors

Loss of block Lock (LOBL)	Set after 65 invalid sync header (00 or 11) in a 1024 window. Reset after 64 consecutive valid 66B sync headers are received (01 or 10).
Loss of Alignment Marker Lock (LOAML)	Set after 4 consecutive marker values are received that do not match the alignment marker that the lane is currently locked to. Reset after 2 valid alignment markers are received 16384 blocks apart.
Loss of Alignment (LOA)	Set if any of the PCS lanes are out of alignment marker lock or the incoming lanes skew exceeds the deskew compensation tolerance.
High BER	The number of invalid sync headers within the current 1.25 ms (40GBase-R) or 500 micro-sec (100GBase-R) equals or exceeds 97.
Invalid Sync Header (ISH)	Set if an invalid sync header (00 or 11) is received.
Invalid Alignment Marker (IAM)	Set if the received alignment marker does not match one of the alignment marker standard encodings excluding BIP3 and BIP7 fields.
BIP	PCS lane bit-interleave parity error.

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